

FIG. 1A

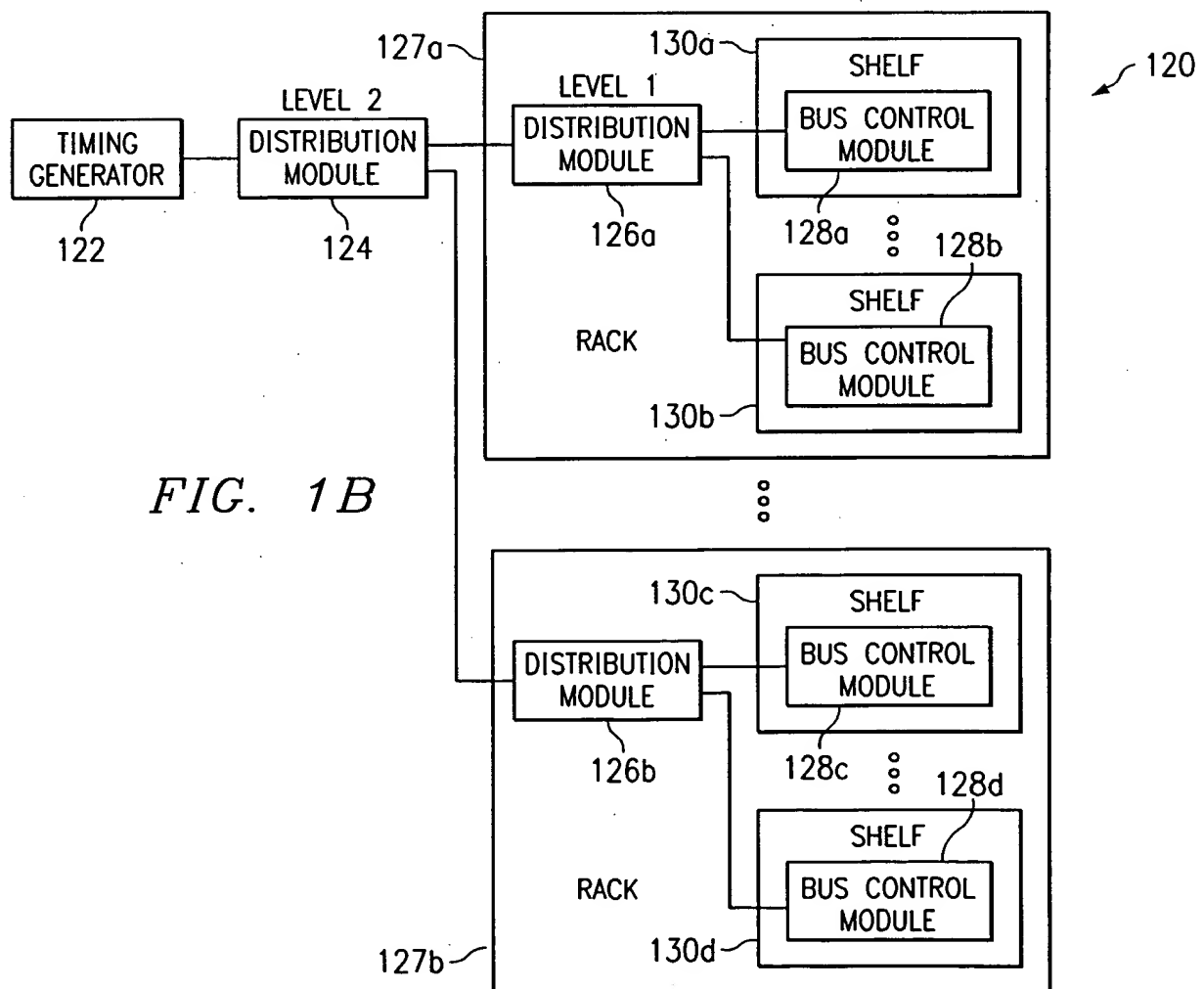
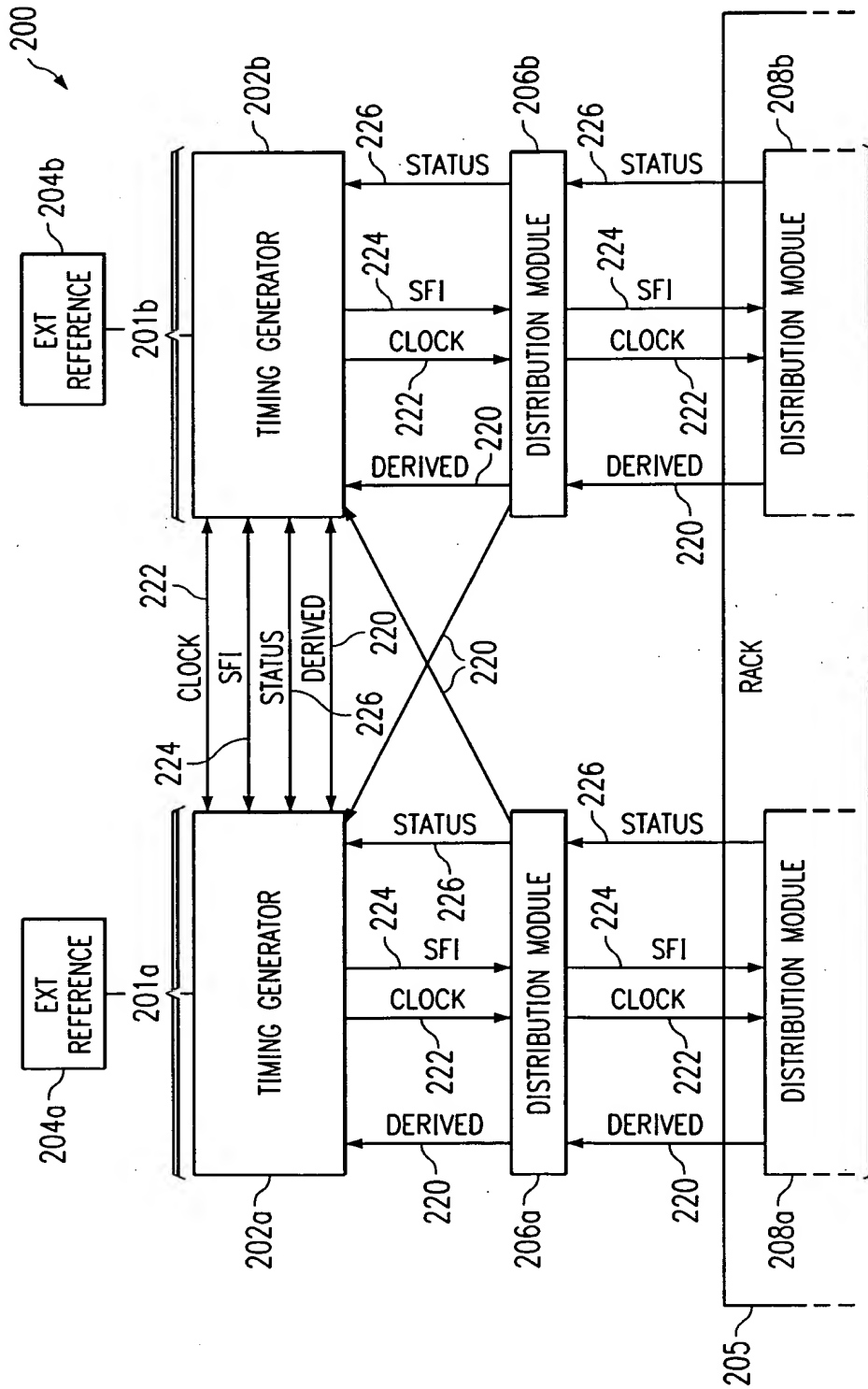


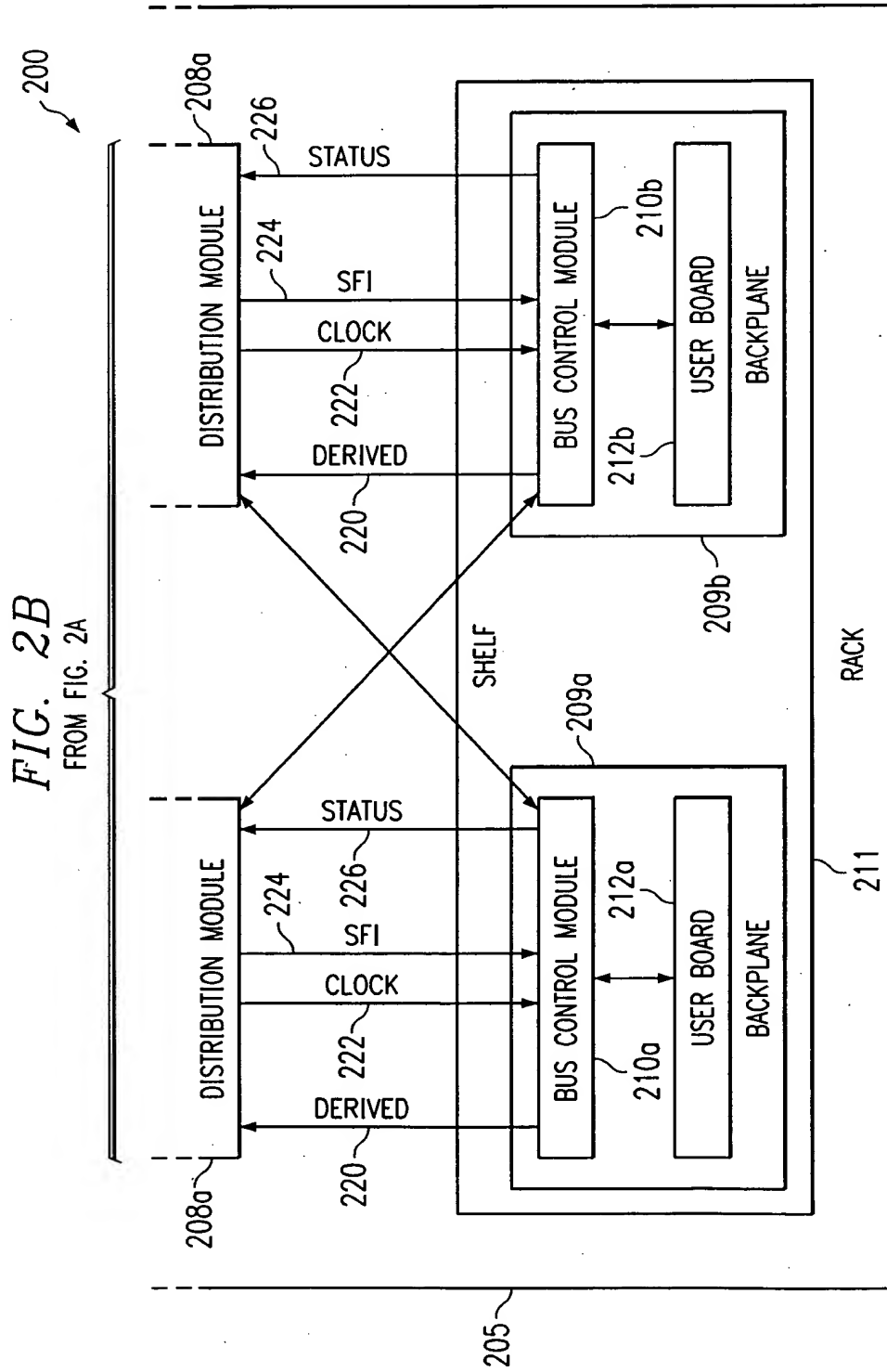
FIG. 1B



TO FIG. 2B

FIG. 2A

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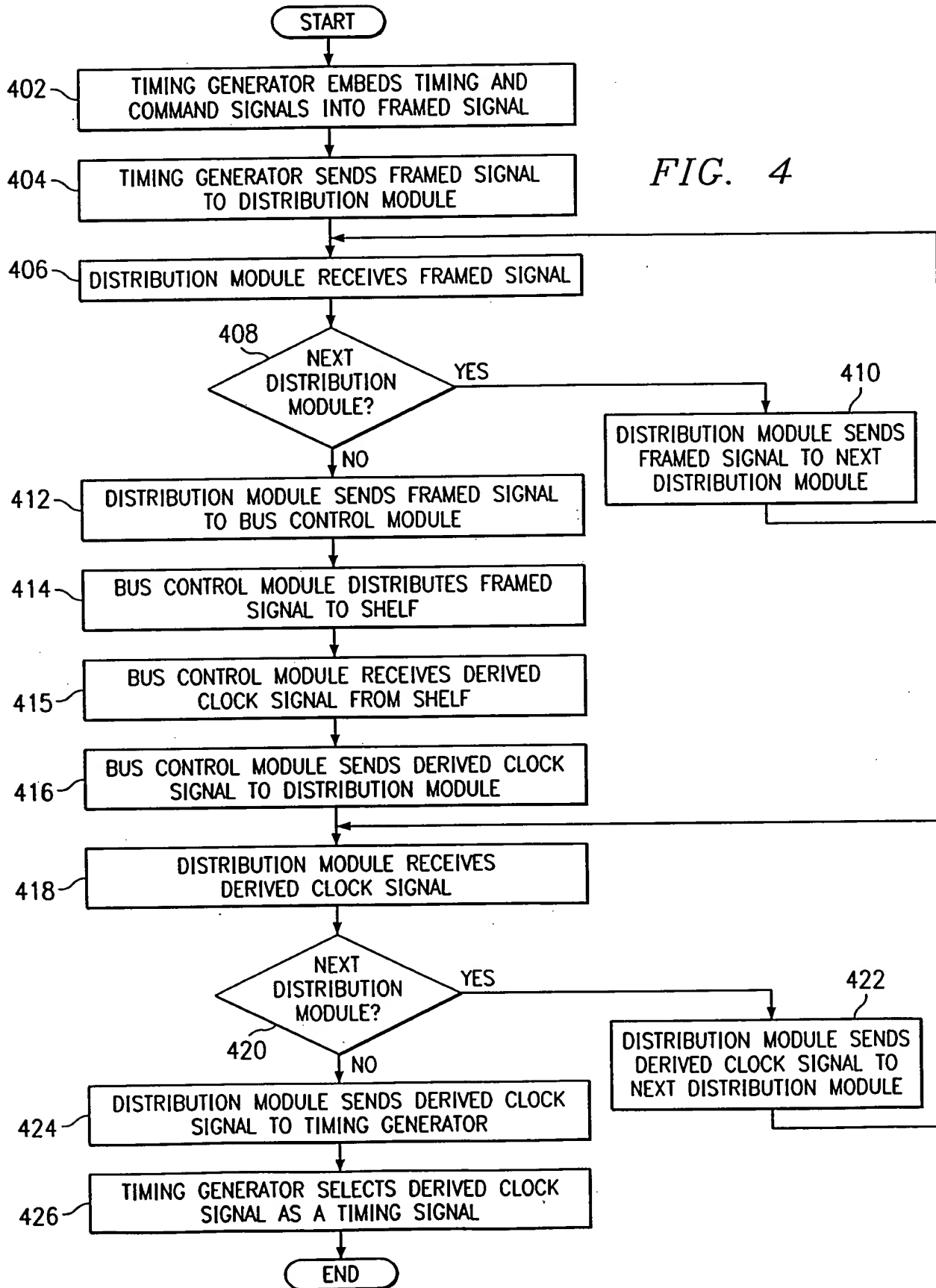
**FIG. 3**

```
graph TD
    301[CONTROLLING PROCESSOR] --- 302[PROCESSOR]
    302 --- 304[TOD]
    302 --- 308[SELF TEST ALARM]
    302 --- 310[DEBUG]
    302 --- 322[CLOCK]
    304 --- 320[SELECTOR 320]
    320 --- 312[DS1/E1]
    320 --- 314[SINE WAVE]
    320 --- 316[COMP]
    320 --- 318[DERIVED CLOCK]
    320 --- 328[GENERATOR]
    328 --- 330[TEST]
    322 --- 334[EXT OSC]
    322 --- 324[FRAMING]
    322 --- 326[COMP CLOCK]
    324 --- 332[TONE]
    324 -- SFI STATUS --> SFI_STATUS[SFI STATUS]
    324 -- STATUS --> STATUS[STATUS]
```

```

graph TD
    START([START]) --> 502[PROCESSOR SENDS SELECTION COMMAND]
    502 --> 504[SELECTOR SELECTS DERIVED SIGNAL]
    504 --> 506[CLOCK USES DERIVED SIGNAL AS TIMING SIGNAL]
    506 --> 508[FRAMING MODULE EMBEDS TIMING SIGNAL IN FRAMED SIGNAL]
    508 --> 510[FRAMING MODULE DISTRIBUTES FRAMED SIGNAL TO DISTRIBUTION NETWORK]
    510 --> 512[FRAMING MODULE RECEIVES STATUS SIGNAL]
    512 --> 514[PROCESSOR RECEIVES STATUS SIGNAL]
    514 --> 516{CHANGE TIMING SIGNAL?}
    516 -- YES --> 504
    516 -- NO --> END([END])

```



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